PG DISSERTION (2017-18)

Sr. No	Roll No	Student's Name	Dissertation Title	Guide	External Guide
1	P16EC001	YATEESH DASILA	Design and Implementation of Acquisition and Tracking Algorithm for Navlc L5 Band Signal	S. N. Shah	Dr. Himanshu Soni, Principal, Vallabh Vidyanagar Anand, Gujarat
2	P16EC002	SHABAD SHASHIDAR REDDY	Study and Implementation of Advertising Extension Feature on Bluetooth Controller	S. Gupta	Dr. Tarun Kumar Gupta, Asst. Prof., MANIT, Bhopal
3	P16EC003	RASHMITHA REDDY M.	Simultaneous Multi Threading Verification Support for Power Management Unit & Improve Coverage Using Machine Learning Tool	S. N. Shah	Dr. Tarun Kumar Gupta, Asst. Prof., MANIT, Bhopal
4	P16EC004	ASHUTOSH KUMAR SINHA	Automatic Engine for Power Measurement in Bluetooth	G. Santra	Dr. Dhaval Pujara, Professor, Nirma Uni., Ahmedabad
5	P16EC005	SHARMA AMITKUMAR S.	Design and Performance Analysis of Next Generation Passive Optical Networks	P. N. Patel	Dr. Dhaval Pujara, Professor, Nirma Uni., Ahmedabad
6	P16EC006	KHOBRAGADE ASHISH	Media Hardware Validation with Efficient Coverage Analysis of Decoder Clips	A.S. Mandloi	Dr. Sunil M. Patel, Assistant Professor, M.S. University, Baroda
7	P16EC007	GYAN SAGAR BARIK	Miniaturized Circular Patch Antenna for WLAN and WiMax Applications	G. Santra	Dr. Dhaval Pujara, Professor, Nirma Uni., Ahmedabad
8	P16EC008	NITIN EKNATH GARDE	Design and Performance Analysis of Hybrid Reconfigurable Antenna for Wireless Application	P.N. Patel	Dr. Prabhat Kumar Sharma, Asst. Prof., VNIT, Nagpur
9	P16EC009	SHASHI RANJAN	Integrating Spectral and Spatial Feature for Hyperspectral Image classification with a Modified Composite Kernel Framework	J. N. Sarvaiya, J. N. Patel	Dr. Suman Mitra, Professor, DA-IICT,, Gandhinahar 382007
10	P16EC010	TAILOR PAWAN K.	Analysis of 5-Gbps Optical System with WDM and Splitters using DCF	A.S. Mandloi	Dr. Prabhat Kumar Sharma, Associate Professor, VNIT, Nagpur
11	P16EC011	SHIV KUMAR YADAV	Performance Analysis of Detection Techniques in MIMO System	S. Gupta	Dr. Prabhat Kumar Sharma, Associate Professor, VNIT, Nagpur
12	P16EC012	KALE KIRAN S.	Optimum filter Design for Cyclostationary Signal in Noise Background	P. K. Shah	Prof. V. Y. doshi, Head & Asso. Prof., Elect. Engg. Deptt., GEC Bharuch
13	P16EC013	GHODESWAR ASHISH B.	Design and Implementation of Modified Planner Fit Method for Grid Based Ionodelay Model for L5 and S Band	S.N. Shah	Dr. Himanshu Soni, Principal, Vallabh Vidyanagar Anand, Gujarat
14	P16EC014	HARSHIT KANOUJIA	Pre-Silicon Register Transfer Level (RTL) Verification of Display Phy IP	A. S. Mandloi	Dr. Tarun Kumar Gupta, Asst. Prof., MANIT, Bhopal
15	P16EC015	CHANDRAVIJAY BHARATI	Miniaturized Koch-snowflake Fractal Antenna with Slots and Parasitic Patches	G. Santra	Dr. Dhaval Pujara, Professor, Nirma Uni., Ahmedabad
16	P16EC017	VALVI JIGNESHKUMAR R.	2-D Systems Modelling and Implementation for Applications in finance	P. K. Shah	Prof. V. Y. doshi, Head & Asso. Prof., Elect. Engg. Deptt., GEC Bharuch

17	P16EC018	AMIT MEHTA	Bluetooth Low Energy (BLE) Mesh-Study and Implantation of MESH Features and Light Model	U. D. Dalal	Dr. Himanshu Soni, Principal, Vallabh Vidyanagar Anand, Gujarat
18	P16EC021	MAHESH G.	Simulation of Switching Between Optical and Acoustic Communication in Underwater Networks	U. D. Dalal	Dr. Himanshu Soni, Principal, Vallabh Vidyanagar Anand, Gujarat
19	P16VL004	LADDA PRIYANKA R.	Validation and Verification of Perfomance Efficient Graphics Architecture	P.J. Engineer	Prof. Joycee Mekie, Assit. Prof., IIT, Gandhinagar
20	P16VL006	KAKANI RAMA KRISHNA	Creation of Faster Environment for Early Verification	A.D. Darji	Dr. Virendra Singh, Professor, EED, IIT Bombay
21	P16VL007	CHELLI VIJAYA	Design Automation to Optimize IEEE Std. 1687 Access Networks for Concurrent Schedule	A.D. Darji	Dr. Virendra Singh, Professor, EED, IIT Bombay
22	P16VL008	ANURAG KUMAR M.	Design and VHDL Implementation of Turbo Codes and Optimization of its Error Correction Capability	M.C.Patel	Prof. Hiren Mewada, Associate Professor, C.S. Patel Inst. of Tech., Changa
23	P16VL009	DUBAKULA KETAVANYA	Automation of Timing Quality Checks and Optimization	A.D. Darji	Dr. Lava Bhargava, Professor, MNNIT, Jaipur
24	P16VL010	WAGHMODE AMOL A.	RTL Design of Datapath of SERDES for On Chip Transceivers	Z.M. Patel	Dr. Biswajit Mishra
25	P16VL011	ANSARI HARIS	VLSI Design and Implementation of an ALU optimized for area and power	Z.M. Patel	Dr. Biswajit Mishra
26	P16VL012	RITHWIJ K.	Enabling UVM Based Test-bench development for Media fixed function units	Z.M. Patel	Dr. Biswajit Mishra
27	P16VL015	VEMPATI CHARAN TEJA	Timing Closure Techniques to fir hold Violation of Near Threshold Voltage Circuits	A.D. Darji	Dr. Lava Bhargava, Professor, MNNIT, Jaipur
28	P16VL016	GAURAV GAUTAM	FIR Filter Design using Wallace Multiplier with Common Boolean Logic Based Square Root Carry Select Adder	P. K. Shah	Prof. V. Y. doshi, Head & Asso. Prof., Elect. Engg. Deptt., GEC Bharuch
29	P16VL017	PATEL DIVYESHKUMAR S.	FPGA Implementation of Software Defined Networking with Open Flow	P.J. Engineer	Prof. Joycee Mekie, Assit. Prof., IIT, Gandhinagar
30	P16VL018	MEGHA PATEL	Simulation of Quantum Dot Based Single Electron Transistor Using TCAD	R.N. Dhavse	Dr. Amit Joshi, Asst., Prof., ECED, MNIT, Jaipur
31	P16VL019	KESHAV A. PATIL	Simulation of Multi Tunnel Junction Single Electron Transistor	R.N.Dhavse	Dr. Amit Joshi, Asst., Prof., ECED, MNIT, Jaipur