PG DISSERTION (2018-19)

Sr. No	Roll No	Student's Name	Dissertation Title	Guide	External Guide
1	P17EC001	SHEKHAR KUMAR YADAV	Compressed sensing with low coherence measurement matrix and sparse dictionary learning	Dr. J. N. Patel	Prof. Tanish Zaveri
2	P17EC002	AVHAD PRATIK AJIT	Design of Fractal and Metamaterial Based Wearable Antenna	Dr. U. D. Dalal	Dr. Sanjeev Gupta
3	P17EC003	RAHUL KUMAR GUPTA	Video deblurring using multi scale deep neural network	Dr. K. P. Upla	Dr. Rakesh Patel
4	P17EC004	SANDHU SIMRAN GURJITSING	Base Station Location and Coverage Optimization using QGIS	Dr. S. N. Shah	Dr. Nikhil Kothari
5	P17EC005	NITESH KUMAR CHAHAR	Performance Analysis of FSO Link Using Multiple Tx/Rx and Aperture Averaging for Different Weather Conditions	Dr. A. S. Mandloi	Dr. D. K. Kothari
6	P17EC006	LAKHLANI SHREEJA DIPAK	Link adaptation in wireless networks using reinforcement learning	Dr. K. P. Upla	Dr. Rakesh Patel
7	P17EC007	KIRTI DATTA	Moving object detection using singular value decomposition approach for slow moving objects	Dr. J. N. Patel	Prof. Tanish Zaveri
8	P17EC008	ZAHABIYA KHEDAWALA	Deep Learning Based Decoder Architecture for Error Correcting codes	Dr. K. P. Upla	Dr. Rakesh Patel
9	P17EC009	DISHTI TIWARI	Unified Diagnostic Services (UDS) based Electronic Control Unit (ECU) Reprogramming and Remote Flashing.	Dr. S. N. Shah	Dr. Nikhil Kothari
10	P17EC010	VASIMALLA YESUDASU	Modelling and Performance Analysis of Surface Plasmon Resonance Based Optical Biosensors	Dr. P. N. Patel	Dr. Hitesh Pandya
11	P17EC011	RAKESH KUMAR CHAUDHARY	Analysis of Detection Techniques in MIMO and Massive MIMO	Dr. S. Gupta	Dr. D. K. Kothari
12	P17EC012	THOKE ADITYA RAJENDRA	Design and Fabrication of compact Multiband Antenna	Dr. P. N. Patel	Dr. Hitesh Pandya
13	P17EC013	RATHOD AJAY GULAB	Realization of Reflective SOA Based DWDM Bidirectional FSO System	Dr. S. Gupta	Dr. D. K. Kothari
14	P17EC014	RENU	Ionospheric Plasma Bubbles based on α-μ Distribution Mode	Dr. S. N. Shah	Dr. Nikhil Kothari
15	P17EC015	CHINTHAKUNTA PARMESH	Numerical and Experimental Analysis of Porous Silicon Based Capacitive Sensors Devices	Dr. P. N. Patel	Dr. Hitesh Pandya
16	P17EC017	YOGESH KUMAR	Realization of High Data Rate Combinational Circuit Using All-Optical Logic Gates	Dr. S. Gupta	Dr. D. K. Kothari
17	P17VL002	SUMAN PANDIT	Design Automation Using Eldo Tool for Efficient & Faster Design of Clock Cells	Dr. P. J. Engineer	Prof. S. M. Patel
18	P17VL003	JAWALE SHUBHANGI C.	Performance optimization design methodology for a functional block	Prof. P. K. Shah	Dr. Preetida Jani

19	P17VL004	ADITYA KORADA	Routing Optimization of VLSI System Layout for Delay Reduction	Dr. Z. M. Patel	Dr. Usha Mehta
20	P17VL005	BARWA NEHA NAYANKUMAR	Interconnect optimization technique for timing convergence in high speed VLSI designs	Dr. Z. M. Patel	Dr. Usha Mehta
21	P17VL006	DEEPAK KUMAR	FPGA Validation of Different Short Codelength QC-LDPC Decoder	Dr. P. J. Engineer	Prof. Rajbabu Velmurugan
22	P17VL008	GAGARE NAMRATA BHAU	Rate Adaptation in 802.11n and 802.11ac by varying link parameters	Dr. J. N. Sarvaiya	Prof. Tanish Zaveri
23	P17VL009	GAYATRI SARIPALLI	Noise Reduction in ECG Signals	Dr. A. D. Darji	Dr. Tanmay D. Pawar
24	P17VL010	BOBBILI SAGAR	Design Automation of Optimize IEEE Std. 1687 On chip Instrument Access Networks	Prof. M. C. Patel	Dr. Mihir V. Shah
25	P17VL011	AKANKSHA SINGH	Designing and optimizing the functional unit block to improve timing & power	Prof. P. K. Shah	Dr. Preetida Jani
26	P17VL012	RAJOO KUMAR GUPTA	Pre-Silicon Functional Verification Strategy of FPML16 of Execution Unit (EU) of Intel CORE CPUs	Prof. P. K. Shah	Dr. Preetida Jani
27	P17VL014	CHANDRAPRAKASH SUWALAKA	VLSI Implementation of Reconfigurable FFT/IFFT Processor for OFDM systems	Dr. Z. M. Patel	Dr. Usha Mehta
28	P17VL015	RATNADEEP PATIL			
29	P17VL016	PRAVEEN	Implementation of Low Power VLSI DCT Architecture for Wireless Capsule Endoscopy	Dr. A. D. Darji	Dr. Tanmay D. Pawar
30	P17VL017	VISHWAJEET S B	High Performance DCT Architecture for HEVC	Dr. A. D. Darji	Dr. Tanmay D. Pawar
31	P17VL018	RAJESH KUMAR	Optimized Packet Classification for Software Defined Networking (SDN)	Prof. M. C. Patel	Prof. S. M. Patel
32	P17VL019	WILFRED KISKU	Acceleration of DL Based Algorithm (GOTURN) on Zynq SoC Using VivadoTM HLS	Dr. P. J. Engineer	Prof. Rajbabu Velmurugan
33	P16VL013	Thirumala Nagasuresh	All Digital Delay Locked Loop	Dr. J. N. Sarvaiya, Dr. A. D. Darji	Dr. Usha Mehta
34	P16VL002	Shah Shrinath Shailesh	Performing Pre-Si Verification of Register Based ALU Using UVM	Prof. M. C. Patel	Dr. Mihir V. Shah